Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-8 were previously canceled without prejudice. Please amend claims 9, 11, 13, 15, 17, 18, 20-23, and 25 and add new claims 27-31 as follows:

Claims 1-8 (cancelled)

9. (currently amended): A very long instruction word (VLIW) memory system comprising:

a VLIW memory having a plurality of instruction slots configured for storing VLIWs, each VLIW stored ~~instruction words~~ at an addressable location[[s]] in the VLIW memory, ~~from which~~ with VLIWs ~~may be~~ being fetched from their addressable locations in the VLIW memory for decoding and execution;

said plurality of instruction slots comprising standard width instruction slots ~~for storing~~ wherein the standard width instruction slots store standard width instructions and at least one expanded width instruction slot having a width that is greater than the standard width instruction slots, wherein the expanded width instruction slot ~~used for storing~~ stores an expanded width instruction having a format that is wider than the standard width instructions and the expanded width instruction has a single opcode of contiguous bits; and

the VLIW memory configured for loading said at least one expanded width instruction slot with ~~an~~ the expanded width instruction accessed from a local data memory separate from the VLIW memory.

10. (original): The memory system of claim 9 wherein the plurality of instruction slots comprise a store unit instruction slot, a load unit instruction slot, an arithmetic logic unit (ALU) instruction slot, a multiply accumulate unit (MAU) instruction slot, and a data store unit (DSU) instruction slot.

11. (currently amended): The memory system of claim 10 wherein the store unit instruction slot is an expanded width instruction slot that stores an expanded width store instruction including additional operand addressing bits to extend ~~compute register file~~ an operand addressing range~~, an additional bit to extend address register file addressing, an additional bit to expand an opcode field, or an additional bit to extend a conditional field~~.

12. (previously presented): The memory system of claim 11 wherein said expanded width store instruction supports expansion of a 32 x 32 bit / 16 x 64 bit configurable register file size to a 128 x 32 bit / 64 x 64 bit/ 32 x 128 bit configurable register file size.

13. (currently amended): The memory system of claim 10 where the load unit instruction slot is an expanded width instruction slot that stores an expanded width load instruction of a first format for load immediate operations including additional bits to extend ~~compute register file~~ an operand addressing range~~, a bit to extend address file register addressing, a bit to extend a conditional field or sixteen bits to extend~~ and to extend an immediate field.

14. (previously presented): The memory system of claim 13 wherein said expanded width load instruction supports expansion of a 32 x 32 bit / 16 x 64 bit configurable register file size to a 128 x 32 bit / 64 x 64 bit/ 32 x 128 bit configurable register file size.

15. (currently amended): The memory system of claim 10 where the ALU, MAU and DSU instruction slots are expanded width instruction slots that store expanded width ALU, MAU, and DSU instructions including additional operand addressing bits ~~in each operand field~~ to extend ~~compute register file~~ an operand addressing range~~, a bit to extend an opcode field, or a bit to extend a data type field~~.

16. (previously presented): The memory system of claim 15 wherein said expanded width ALU, MAU, and DSU instructions each supports expansion of a 32 x 32 bit / 16 x 64 bit configurable register file size to a 128 x 32 bit / 64 x 64 bit/ 32 x 128 bit configurable register file size.

17. (currently amended): A very long instruction word (VLIW) instruction memory basket (VIMB) system comprising:

an instruction register for storing a load indirect VLIW (LIV) instruction comprising data address information and a load mask bit field specifying which instruction slots are to be loaded in a VLIW having at least one instruction slot that is an expanded instruction slot, the VLIW accessible from a local data memory, the VLIW to be loaded at an addressable location in the VIMB;

an instruction bit organizer ~~for receiving~~ wherein the instruction bit organizer receives instructions as data from the local data memory according to the data address information and

based on the load mask bit field ~~organizing~~ organizes the bits from the data encoded instructions into proper format ~~for~~ to be ~~loading~~ loaded into the specified instruction slots in the VIMB in response to execution of the LV instruction; and

the VIMB comprising a plurality of VLIWs from which VLIWs may be fetched for execution, wherein the width of the at least one expanded instruction slot is greater than the width of instructions required in program storage.

18. (currently amended): A very long instruction word (VLIW) memory system comprising:

an instruction memory holding a plurality of instructions of a first bit width, the plurality of instructions having at least one execute VLIW instruction that specifies a VLIW address for fetching a VLIW for decoding and execution; and

a very long instruction memory having at least one instruction slot[[s]] for storing an instruction[[s]] of a second bit width having a single opcode of contiguous bits wherein the second bit width is different from the first bit width and wherein the very long instruction memory holds VLIWs at addressable locations, ~~that~~ the VLIW having the instruction of the second bit width being ~~may be~~ fetched from the very long instruction memory at the VLIW address as a result of executing the at least one execute VLIW instruction.

19. (previously presented): The system of claim 18 wherein instructions of the second bit width are stored in a data memory and delivered to the very long instruction memory utilizing a data bus.

20. (currently amended): A very long instruction word (VLIW) memory system comprising:

a plurality of instruction slots for storing instruction words forming a VLIW, at least one of said plurality of instruction slots having a compressed format for storing a compressed instruction having a narrower instruction format with respect to an instruction format of a standard width required by program instructions stored in a program storage, wherein the VLIW resides at an addressable location in a VLIW memory separate from the program storage, the VLIW memory holding VLIWs that may be fetched for execution; and

means for loading said at least one compressed format slot with a compressed instruction.

21. (currently amended): A processing apparatus comprising:

a memory for storing a processing apparatus program comprising short instruction words;

an indirect very long instruction word (VLIW) memory comprising a plurality of instruction slots for storing instruction words, at least one of said instruction slots having an expanded instruction format sized according to execution function and operand storage capacity and independent of the size of the short instruction words, wherein the expanded instruction format comprises a single opcode of contiguous bits and the plurality of instruction slots are organized to form a plurality of VLIWs and each VLIW resides at an addressable location in the indirect VLIW memory, the indirect VLIW memory holding VLIWs that may be fetched for execution;

at least one data memory unit storing instruction operands; and

at least two execution units for executing an expanded VLIW having an instruction of an expanded instruction format, the expanded VLIW fetched from the indirect VLIW memory at a VLIW address generated in response to an execute VLIW short instruction word dispatched from the memory.

22. (currently amended): The processing apparatus of claim 21 wherein the short instruction words each comprises a first width of K-bits and the expanded instruction format comprises a second width of T-bits, wherein T≠K.

23. (currently amended): The processing apparatus of claim ~~22~~ 21 wherein the short instruction word comprises at least one operand address field of A-bits and the expanded instruction format comprises at least one operand address field of B-bits ~~supporting direct operand addressing~~, wherein B > A.

24. (original): The processing apparatus of claim 23 wherein the data memory unit has a capacity 2^B data values.

25. (currently amended): The processing apparatus of claim 21 wherein at least one of the at least two execution units operates ~~on a slot instruction format~~ in response to the single opcode and directly accesses operands from the data memory unit for execution.

26. (previously presented): The processing apparatus of claim 21 wherein the at least two execution units operate as two execution units when executing two VLIW memory slot instructions as specified by a two slot execute indirect VLIW instruction, and wherein the at least two execution units operate as one execution unit when executing one VLIW memory slot instruction as specified by a one slot execute indirect VLIW instruction.

27. (new): The memory system of claim 9 wherein the standard width instructions are each formatted to have a width that fits in an addressable location in an instruction memory without crossing an addressing boundary, the instruction memory separate from the VLIW memory.

28. (new): The memory system of claim 9 wherein the expanded width instruction is loaded into the at least one expanded width instruction slot under control of a load VLIW instruction that is a standard width instruction, the load VLIW instruction providing local data memory address information that is used to access the expanded width instruction from the local data memory for loading in the VLIW memory.

29. (new): The memory system of claim 9 wherein the expanded width instruction is accessed from a local data memory at a data address generated in response to a load VLIW instruction and loaded in the VLIW memory at a VLIW address generated in response to the load VLIW instruction.

30. (new): The VIMB system of claim 17 wherein the expanded instruction slot is loaded under control of the LV instruction, the LV instruction providing VIMB address information that is used to select the addressable location in the VIMB to be loaded with the expanded instruction in the at least one expanded instruction slot.

31. (new): The system of claim 18 wherein the single opcode is decoded to determine the operands to be used in the execution of the instruction of the second bit width.